1. (Amended) A method of manufacturing built-in capacitors in a multi-layer substrate, said method comprising:

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forming a plurality of via holes in said multi-layered substrate, said multi-layered substrate comprising a first dielectric layer, a second dielectric layer, and a third dielectric layer, said second dielectric layer having two second conductive layers being respectively mounted on a top and a bottom surface to pattern as power plane and ground plane, said first dielectric layer, and said third dielectric layer having respectively a first conductive layer and a third conductive layer;

filling a capacitor dielectric material into a portion of said via holes, which are predetermined design as capacitors, said capacitor dielectric material having a dielectric constant substantially higher than said second dielectric layer;

curing said capacitor dielectric material;

masking a dry film on areas of said second conductive layers where those are desired regions to form a copper layer thereon;

etching away exposed regions of said second conductive layers so as to form ground plane and power plane;

removing said dry film;

electroplating two copper layers respectively on said ground plane and power plane to seal said copper dielectric material to form built-in capacitors;

assembling and sintering said first conductive layer, said first dielectric layer, said ground plane, said second dielectric layer, said power plane, said third dielectric layer, and said third conductive layer together;

patterning said first conductive layer and said third conductive layer to form connective trace layers; and

performing a plating through hole process to connect said via holes to said connective trace layers and said power plane and ground plane.